Nested-Adaptive Framework for Islanded DC Microgrid Secondary Control Over Wireless Links

Mohammad Amin Jarrahi and Kamyar Mehran
School of Electronic Engineering and Computer Science (EECS)
Queen Mary University of London, London, United Kingdom
m.jarrahi@qmul.ac.uk and k.mehran@qmul.ac.uk

***Abstract*—This paper proposes a nested-adaptive secondary control framework for islanded DC microgrids operating over wireless links with bounded delay and packet loss. The method combines five elements that are designed to work on different time scales: a distributed consensus secondary controller for voltage restoration and state of charge sharing, a hysteresis event trigger with minimum and maximum inter-event times to reduce transmissions and avoid event accumulation, a controller bank with eight prevalidated parameter modes, a lightweight regime classifier that proposes mode changes from recent electrical and communication features, and a supervisory gate that enforces dwell time, confidence checks, and rollback to a conservative safe mode. A fast Level-0 bounded trim is added to each converter reference at every control tick, with explicit magnitude and slew limits so its effect can be treated as a bounded input to the secondary loop. The approach is evaluated in experimental 380V DC microgrid hardware-in-the-loop (HIL) test-bench with wireless delays in the 10 to 200 ms range and packet loss up to 15%. Across the tested scenarios, the proposed scheme reduces message rate by about 30% to 50% relative to periodic communication while maintaining improved voltage regulation and SoC sharing.**

***Index Terms*—DC microgrids; Secondary Control; Event-Triggered Communication; Wireless Delay; Distributed Consensus Control; SoC balancing**

I. Introduction

Islanded DC microgrids are an enabling technology for remote communities and small islands because they can integrate renewable generation and storage efficiently while avoiding the synchronization requirements of AC systems. Their control is commonly hierarchical [1]. Primary control is implemented locally at each converter to ensure fast stabilization and approximate current sharing, typically through droop characteristics. Secondary control acts on a slower time scale to restore the DC bus voltage to its nominal value and to coordinate sharing objectives such as battery state of charge (SoC) across multiple units. Tertiary control and energy management optimize setpoints over minutes to hours. In practice, secondary control is the layer that most directly depends on communication, and it is therefore the first to degrade when wireless links become unreliable [2].

A practical way to implement secondary control in multi-unit microgrids is distributed secondary control, where each unit uses local measurements and limited neighbor-to-neighbor information exchange rather than a central coordinator [3]. In field deployments, this exchange is often carried by wireless or hybrid links with time-varying delay, packet loss, and bandwidth limits [4]. This creates a persistent trade-off: frequent communication improves coordination and regulation but increases network load and sensitivity to congestion, while reduced communication can degrade voltage restoration, especially during load transients, renewable fluctuations, and under constant power loads that reduce damping [5].

Most distributed secondary controllers assume periodic communication and fixed gains tuned offline, including PI and consensus-based designs [6]. These choices simplify analysis and implementation, but they impose a constant communication burden and their fixed tuning can be brittle when the operating regime or network quality changes. Event-triggered communication reduces transmissions by sending updates only when local innovations exceed thresholds, and hysteresis with a minimum inter-event time avoids chattering and excludes event accumulation. However, many event-triggered schemes still use fixed gains and fixed thresholds, so the regulation-communication trade-off is not adjusted when conditions shift [7]. Learning-based controllers can improve adaptation, but for secondary control they often raise two concerns: maintaining a clear path to enforce run-time safety constraints, and respecting microgrid time scales so that online adaptation does not interact poorly with fast electrical dynamics [8].

This paper addresses these issues with a nested-adaptive secondary control framework. The design aligns adaptation with microgrid time scales and restricts online changes to a testable structure. The baseline is a distributed consensus secondary controller for voltage restoration and SoC sharing. Communication is reduced using an event-trigger with hysteresis and explicit minimum and maximum inter-event times. Adaptation is restricted to a controller bank of prevalidated modes that bundle secondary gains and trigger parameters for representative regimes. A lightweight classifier proposes the mode from recent electrical and communication features, and a supervisor enforces dwell time, confidence gating, and rollback to a conservative safe mode. A fast Level-0 bounded trim layer provides small per-tick reference adjustments with magnitude and slew limits so its effect can be treated as a bounded input to the slower secondary loop. Results are reported for a 380 V islanded DC microgrid under bounded delay and packet loss, supported by a hardware-in-the-loop (HIL) real-time prototype for integration and timing checks. So, the main contributions of the paper can be summarized as:

- A nested-adaptive, computational intelligence-enabled secondary control framework combining bounded fast trim, controller bank selection, and supervised switching.
- Event-triggered distributed secondary control with hys-

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teresis and explicit lower and upper inter-event bounds.
- A safe adaptation mechanism using a data-driven classifier with confidence gating and rollback.
- Experimental HIL validation under wireless delay and packet loss with quantified communication reduction and regulation performance.

II. System Model and Objectives

This section introduces only the plant and communication models required to define the proposed secondary control architecture and its evaluation. In all equations of the paper, we consider the following notations with the mentioned units: i_i (A), v_{dc} (V), L_i (H), r_i (Ω), C_{dc} (F).

A. DC Microgrid and Primary Droop

Consider an islanded DC microgrid with n converter-interfaced distributed energy resource units (DERUs) connected to a common DC bus. A compact averaged model that captures the dominant bus-voltage dynamics is [9]:

$$\begin{aligned} L_i\dot{i}_i(t) &= v_i^{\mathrm{ref}}(t) - v_{\mathrm{dc}}(t) - r_i i_i(t), \quad i = 1,\dots,n \\ C_{\mathrm{dc}}\dot{v}_{\mathrm{dc}}(t) &= \sum_{j=1}^{n} i_j(t) - i_L(v_{\mathrm{dc}}(t)), \end{aligned} \tag{1}$$

where i_i is the output current of unit i, v_{dc} is the common bus voltage, L_i and r_i model the converter output filter, C_{dc} is the equivalent bus capacitance, and $i_L(\cdot)$ is the aggregate load current. Primary control is implemented via a voltage-current droop law augmented by secondary correction and a bounded fast trim:

$$v_i^{\mathrm{ref}}(t) = V_{\mathrm{ref}} + u_i(t) + \Delta v_i(t) - m_i i_i(t). \tag{2}$$

Each term in (2) has the following role:

- V_{ref} is the nominal DC bus voltage reference.
- $u_i(t)$ is the secondary control signal that restores v_{dc} and coordinates sharing objectives across DERUs.
- $\Delta v_i(t)$ is a fast bounded trim applied at the converter level to improve transient response while remaining magnitude- and slew-limited.
- $m_i i_i(t)$ is the droop term that provides decentralized current sharing and stabilizing negative feedback at the primary layer, where $m_i > 0$ is the droop coefficient.

For completeness, each DERU is assumed to include a battery with $\mathrm{SoC}_i \in [0,1]$ whose slow dynamics can be approximated by:

$$\dot{\mathrm{SoC}}_i(t) = -\frac{\eta_i P_{b,i}(t)}{E_{\mathrm{cap},i}}, \tag{3}$$

where $P_{b,i}(t)$ is battery power (positive when discharging), η_i is efficiency, $E_{\mathrm{cap},i}$ is energy capacity and $\mathrm{SoC}i \in [0,1]$ is the normalized state of charge (dimensionless).

B. Wireless Communication Model

Information exchange among DERUs occurs over a directed communication graph $\mathcal{G} = (\mathcal{V}, \mathcal{E})$ with node set $\mathcal{V} = \{1,\dots,n\}$ and directed edges $\mathcal{E} \subseteq \mathcal{V} \times \mathcal{V}$. The neighborhood of node i is $\mathcal{N}_i = \{j \mid (j,i) \in \mathcal{E}\}$. Each DERU transmits an information vector that includes its secondary variable and SoC:

$$y_j(t) = \begin{bmatrix} u_j(t) \\ \mathrm{SoC}_j(t) \end{bmatrix}. \tag{4}$$

Due to wireless delay and loss, node i does not access $y_j(t)$ directly but instead uses delayed and held values,

$$\tilde{y}_{j\to i}(t) = \begin{cases} y_j(t - \tau_{ij}(t)), & \text{if a packet is received,} \\ \tilde{y}_{j\to i}(t^-), & \text{if a packet is lost} \end{cases} \tag{5}$$

where $\tau_{ij}(t)$ is a time-varying delay on link (j,i) satisfying:

$$0 \le \tau_{ij}(t) \le \tau_{\max}, \tag{6}$$

and $\tilde{y}_{j\to i}(t^-)$ denotes the last successfully received value held by a sample-and-hold mechanism. In implementation, node i uses $\hat{u}_j(t)$ and $\widehat{\mathrm{SoC}}_j(t)$ extracted from $\tilde{y}_{j\to i}(t)$, that is:

$$\tilde{y}_{j\to i}(t) = \begin{bmatrix} \hat{u}_j(t) \\ \widehat{\mathrm{SoC}}_j(t) \end{bmatrix}. \tag{7}$$

Packet loss is modeled as a Bernoulli process per link with loss probability bounded by $p_{\max}$; when loss occurs, the held value is used until the next successful reception or until a forced-update rule (defined later by the event trigger) applies.

C. Control Objectives and Metrics

The secondary control problem considered in this paper has three objectives:

a) Voltage restoration: Restore the common bus voltage to the nominal value:

$$\lim_{t\to\infty} v_{\mathrm{dc}}(t) = V_{\mathrm{ref}}. \tag{8}$$

b) SoC balancing: Drive the battery SoC to a common value across DERUs:

$$\lim_{t\to\infty} (\mathrm{SoC}_i(t) - \mathrm{SoC}_j(t)) = 0, \quad \forall i,j \in \mathcal{V}. \tag{9}$$

c) Reduced transmissions: Reduce the number of wireless transmissions relative to a periodic communication baseline while maintaining acceptable regulation and sharing performance.

To evaluate performance in experiments, the following metrics are reported over a horizon $[0,T]$ [10]:

- RMS voltage error (%):

$$e_{\mathrm{rms}}(\%) = 100\sqrt{\frac{1}{T}\int_0^T \left(\frac{v_{\mathrm{dc}}(t) - V_{\mathrm{ref}}}{V_{\mathrm{ref}}}\right)^2 dt}. \tag{10}$$

- Maximum voltage deviation (p.u.):

$$e_{\max}(\text{p.u.}) = \max_{t\in[0,T]} \left|\frac{v_{\mathrm{dc}}(t) - V_{\mathrm{ref}}}{V_{\mathrm{ref}}}\right|. \tag{11}$$

- Settling time: Given a tolerance band $\pm\epsilon_v$ (p.u.), the settling time is

$$T_s = \inf\left\{t_0 \,\middle|\, \left|\frac{v_{\mathrm{dc}}(t) - V_{\mathrm{ref}}}{V_{\mathrm{ref}}}\right| \le \epsilon_v,\ \forall t \ge t_0\right\}. \tag{12}$$

- SoC spread (%):

$$\Delta_{\mathrm{soc}}(\%) = 100 \max_{t\in[0,T]} \left(\max_i \mathrm{SoC}_i(t) - \min_i \mathrm{SoC}_i(t)\right). \tag{13}$$

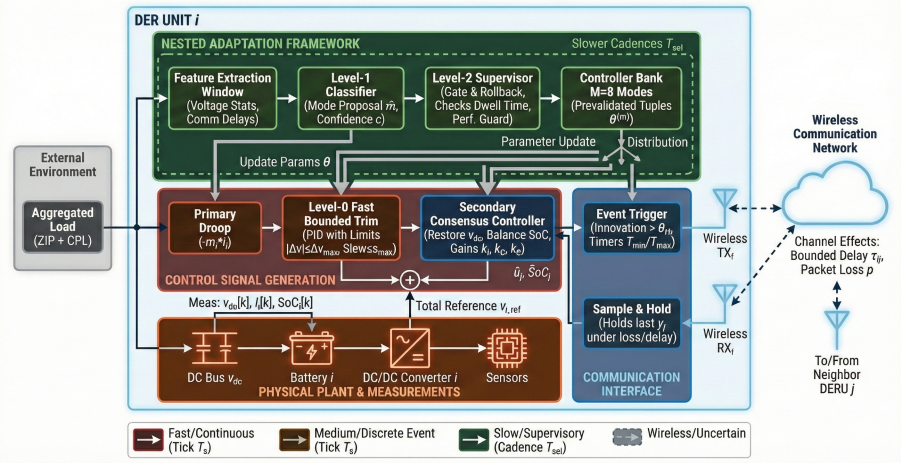

Fig. 1. Proposed nested-adaptive secondary control architecture with event-triggered communication.

- Communication rate reduction (%): With $N_{\mathrm{tx}}^{\mathrm{per}}$ transmissions under periodic communication and $N_{\mathrm{tx}}^{\mathrm{evt}}$ under event-triggered communication over $[0, T]$,

$$R_{\mathrm{comm}}(\%) = 100\left(1 - \frac{N_{\mathrm{tx}}^{\mathrm{evt}}}{N_{\mathrm{tx}}^{\mathrm{per}}}\right). \tag{14}$$

III. Proposed Method

This section presents the proposed control framework. The design starts from a standard consensus-based secondary integrator and adds five elements: (i) an event-triggered communication policy with hysteresis and timing constraints, (ii) a fast bounded trim injected at the voltage reference, (iii) a finite controller bank with $M = 8$ prevalidated modes, (iv) a lightweight regime classifier that proposes a mode, and (v) a supervisor that gates switching and provides rollback. The resulting structure separates adaptation across three nested time scales: milliseconds (Level-0 trim), seconds (mode proposal), and tens of seconds to minutes (supervision). The system model in Section II is continuous-time, while the implemented controller operates in discrete time with sampling period T_{samp}.

A. Architecture Overview

Figure 1 summarizes the signal flow. Each converter applies primary droop and receives two additive terms: the secondary correction $u_i[k]$ and the fast trim $\Delta v_i[k]$. The secondary state $u_i[k]$ is updated by a distributed consensus integrator that depends on local voltage error and neighbor information. Neighbor information is exchanged using the event-triggered policy by transmitting secondary variable and SoC as Eq. (4) and storing the last transmitted value $\hat{y}_i[k]$. Online adaptation is constrained to selecting among a finite set of parameter tuples $\{\theta^{(m)}\}_{m=1}^{8}$ in a controller bank. The regime classifier proposes a mode index m using features extracted from recent electrical measurements and communication statistics. The supervisor accepts or rejects mode changes based on dwell time, confidence, and simple performance guards, and can roll back to a conservative safe mode if sustained degradation is detected.

B. Baseline Consensus Secondary Update

Let $u_i[k]$ denote the secondary correction of unit i at sampling time k with sampling period T_{samp}. Using local bus-voltage measurement and delayed or held neighbor information, the baseline distributed update is:

$$\begin{aligned} u_i[k+1] = u_i[k] &- T_s k_{I,i}\, e_v[k] \\ &- T_s k_{C,i} \sum_{j \in \mathcal{N}_i} a_{ij}\big(u_i[k] - \hat{u}_j[k]\big) \\ &- T_s k_{S,i} \sum_{j \in \mathcal{N}_i} a_{ij}\big(\mathrm{SoC}_i[k] - \widehat{\mathrm{SoC}}_j[k]\big), \end{aligned} \tag{15}$$

where $e_v[k] = v_{\mathrm{dc}}[k] - V_{\mathrm{ref}}$, $a_{ij} > 0$ are communication weights, and $\hat{u}_j[k]$, $\widehat{\mathrm{SoC}}_j[k]$ are the most recently received neighbor values held under delay and loss. The first term integrates voltage error to restore v_{dc} to V_{ref}. The second term aligns secondary states through neighbor differences. The third term penalizes SoC mismatch to promote SoC balancing.

C. Event-Triggered Communication With Hysteresis

Each unit maintains the transmitted vector $y_i[k]$ and its last transmitted value $\hat{y}_i[k]$ as:

$$z_i[k] = \|y_i[k] - \hat{y}_i[k]\|_2 . \tag{16}$$

Let t_i^{last} be the time of the last successful transmission of unit i. Two thresholds $\theta_H > \theta_L > 0$ and two timing constants $T_{\min} > 0$ and $T_{\max} > T_{\min}$ are used. So, the transmission policy is:

- Holdoff (no transmission allowed):

$$t - t_i^{\mathrm{last}} < T_{\min}. \tag{17}$$

- Forced update (avoid stale information):

$$t - t_i^{\mathrm{last}} > T_{\max}. \tag{18}$$

- Otherwise, trigger if:

$$z_i[k] > \theta_H. \tag{19}$$

TABLE I
CONTROLLER BANK STRUCTURE BUILT FROM THREE BINARY REGIME AXES.

Regime axis	Categories used in bank
Communication quality	good, poor
CPL severity	low, high
SoC imbalance	low, high

After a transmission, set $\hat{y}_i[k] \leftarrow y_i[k]$ and update $t_i^{\text{last}} \leftarrow t$. Re-arm only when:

$$z_i[k] < \theta_L. \tag{20}$$

The hysteresis pair (θ_H, θ_L) reduces chattering. The minimum inter-event time $T_{\min}$ prevents event accumulation. The maximum silence time $T_{\max}$ bounds how stale neighbor data can become.

D. Level-0 Fast Bounded Trim

Level-0 applies a small reference trim $\Delta v_i[k]$ at each control tick. The trim is designed to be explicitly bounded so that it can be treated as a bounded input acting on slower secondary loop. A simple filtered proportional derivative form is:

$$\Delta v_i[k] = \text{sat}_{\Delta v_{\max}}\Big(\beta\, \Delta v_i[k-1] - k_{p,i}\, e_v[k] - k_{d,i}\, \dot{e}_v[k]\Big), \tag{21}$$

where $\beta \in (0,1)$ is a forgetting factor and $\dot{e}_v[k] = (e_v[k] - e_v[k-1])/T_s$. The saturation enforces:

$$|\Delta v_i[k]| \le \Delta v_{\max}. \tag{22}$$

A slew limit is also enforced:

$$|\Delta v_i[k] - \Delta v_i[k-1]| \le s_{\max}. \tag{23}$$

Practically, $\Delta v_i[k]$ is a safe micro-adjustment that improves transient behavior while keeping the effect of fast adaptation inside explicit magnitude and rate limits.

E. Controller Bank

Online adaptation of the controller bank is constrained to choosing among eight prevalidated modes. Each mode $m \in \{1, \dots, 8\}$ is defined by a parameter tuple:

$$\begin{aligned}\theta^{(m)} = \big\{&k_{I,i}^{(m)}, k_{C,i}^{(m)}, k_{S,i}^{(m)}, \theta_H^{(m)}, \theta_L^{(m)}, \\ &T_{\min}^{(m)}, T_{\max}^{(m)}, \Delta v_{\max}^{(m)}, s_{\max}^{(m)}, k_{p,i}^{(m)}, k_{d,i}^{(m)}\big\}.\end{aligned} \tag{24}$$

The 8 modes are formed from three binary axes, yielding $2 \times 2 \times 2 = 8$ combinations:

- communication quality: good or poor
- constant power load severity: low or high
- SoC imbalance: low or high

Offline validation follows a three-step engineering pipeline:

1) Define constraints that modes must satisfy (for example, voltage regulation bounds and acceptable damping in the operating region used for tuning).
2) Select representative parameter sets $\theta^{(m)}$ that target the regime combinations in Table I.
3) Validate each mode in nonlinear simulation across representative scenarios; discard or retune modes that violate constraints.

Algorithm 1 Supervisor for mode switching and rollback

```
Inputs: proposal m̂, confidence c, metrics M, active mode m_act
if t − t^mode ≥ T_switch AND c ≥ c_min AND guard(M) is satisfied then
    m_act ← m̂, t^mode ← t
end if
if guard(M) violated for longer than T_r then
    m_act ← m_safe
end if
Apply parameters θ ← θ^(m_act)
```

This bank-based design limits online adaptation to a finite set of tested parameter tuples, which is easier to review and audit than a continuously updating black-box controller.

F. Level-1 Regime Classifier (Mode Proposal)

Level-1 runs every T_{sel} seconds and proposes a mode index $\hat{m}$. It computes a feature vector $\phi[k]$ from a sliding window of recent measurements. The feature set is kept lightweight:

- Voltage-error statistics over the window (mean, RMS, peak)
- SoC residual features (local SoC and differences relative to held neighbor SoC values)
- Communication features (delay and loss summaries, age of neighbor data, recent transmission count)

A small classifier outputs mode probabilities

$$p_m[k] = \text{softmax}_m\big(f_\psi(\phi[k])\big), \quad m = 1, \dots, 8, \tag{25}$$

and proposes:

$$\hat{m}[k] = \arg\max_m p_m[k], \qquad c[k] = \max_m p_m[k], \tag{26}$$

where $c[k]$ is a confidence measure used by the supervisor.

Training is simulation-labeled: for each window, candidate modes are evaluated over a short horizon subject to constraints, and the best feasible mode provides the label for supervised learning.

G. Level-2 Supervisor (Dwell Time, Gate, Rollback)

Level-2 enforces safe and slow switching. Let m_{act} be the active mode and let t^{mode} be the last accepted switching time. A proposed mode change is considered only if a dwell time is satisfied:

$$t - t^{\text{mode}} \ge T_{\text{switch}}. \tag{27}$$

The supervisor also requires classifier confidence $c[k] \ge c_{\min}$ and applies a simple performance guard, for example based on moving RMS voltage error and SoC spread staying within preset limits. If sustained degradation persists for longer than a rollback time T_r, the supervisor forces a switch to a conservative safe mode m_{safe} in the bank. This supervisory layer as presented in Algorithm 1 is intended to make the overall approach testable: mode changes are slow, gated by simple conditions, and a conservative fallback mode is always available.

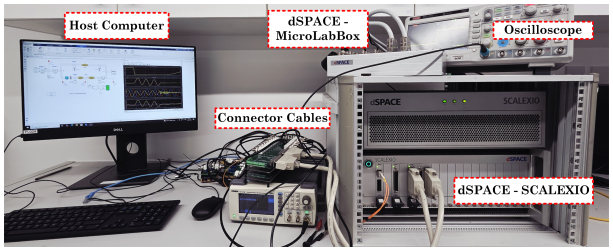

Fig. 2. Developed HIL testbed for experimental analysis

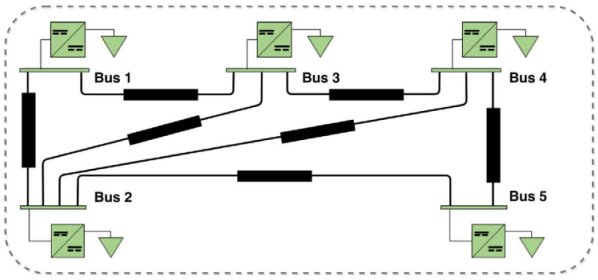

Fig. 3. The 5-bus islanded DC microgrid as studied test system [11]

IV. Experimental HIL Study

This section evaluates the proposed nested-adaptive secondary control with event-triggered communication on a islanded DC microgrid considering two main scenarios.

The HIL setup is shown in Fig. 2. It consists of dSPACE SCALEXIOreal-time simulator for HIL simulation of DC microgrid, dSPACE MicroLabBox for real-time simulation of communication links using TrueTime network modelling framework, and developed multi-agent embedded controllers based on Arduino boards with corresponding signal conditioning inter-face circuits. The HIL platform closely emulates real-world microgrid operation, including embedded controllers, communication delays, and hardware-level timing, and therefore provides a realistic validation environment without requiring field deployment. Controllers that support WiFi communication protocol, have also been connected to the dSPACE SCALEXIO. Moreover, the proposed strategy has been developed using digital signal processing (DSP) instructions of ARM Cortex-M0+, and model-based implementation and measurements have been carried out using MATLAB/Simulink, respectively. A 5-unit, 380 V islanded DC microgrid is simulated as shown in Fig. 3, where each unit is interfaced through a DC/DC converter with primary droop control and the secondary layer described in Section III. More details of the studied dc microgrid can be found in [11]. The secondary update is implemented in discrete time with sampling period T_{samp}. Unless stated otherwise, the communication network is a directed graph that remains strongly connected during the tests, with each unit receiving information from its in-neighbors $\mathcal{N}_i$ and weights a_{ij}.

Wireless communication is modeled with bounded time-varying delay and packet loss. The delay on each link satisfies $10\ \text{ms} \leq \tau_{ij}(t) \leq 200\ \text{ms}$, and packet losses are independent Bernoulli events with probability up to $p_{\max} = 0.15$. When a packet is lost, the last received neighbor value is held

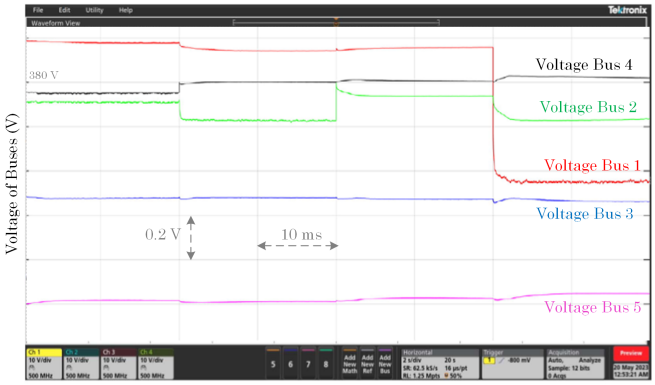

Fig. 4. Scenario 1 (load change, nominal comms): Voltage profiles of buses during the experiment

(sample-and-hold). Loads follow a ZIP model with a constant power load (CPL) portion to represent negative incremental impedance effects. Unless otherwise stated, the CPL portion is kept fixed within the validated operating region used for the controller-bank design. The proposed controller uses 8 modes (controller bank), a regime classifier that proposes mode updates at a slower cadence than T_{samp}, and a supervisor that enforces dwell time and rollback.

A. Scenario 1: Stepwise Load Increase Under Nominal Communication

This scenario evaluates transient voltage regulation and communication savings during a structured stepwise load increase over an 80s experiment window. The total load level is increased in steps of 20% every 20s, covering four operating intervals. The load composition is modeled as ZIP with a fixed CPL fraction, so the disturbance is a change in load magnitude while the load type remains unchanged. Communication conditions are nominal, meaning the wireless delay is bounded and packet loss is low relative to the stressed case in Scenario 2.

Figure 4 shows the DC bus voltages of the monitored buses during the stepwise loading profile. Clear voltage changes are observed at the load-step instants (around $t = 20$s, $t = 40$s, and $t = 60$s), followed by recovery toward the operating level set by V_{ref} and the droop-plus-secondary control structure. In this scenario, the Level-0 bounded trim mainly reduces the peak voltage deviation immediately after each step, while the event-triggered updates reduce message rate once the system returns to a slowly varying regime.

B. Scenario 2: Time-Varying Loads Under Stochastic Communication Delay

This scenario evaluates robustness when the electrical operating point varies continuously and the secondary coordination layer experiences large, time-varying communication delay. Time-varying loads are connected across the buses during an 80 s run, so the DERUs must repeatedly correct the bus voltages while tracking changing power demand. Meanwhile, the inter-controller communication delay is modeled as a random Gaussian process with an average value of 200 ms. Each agent applies the most recently received neighbor information under

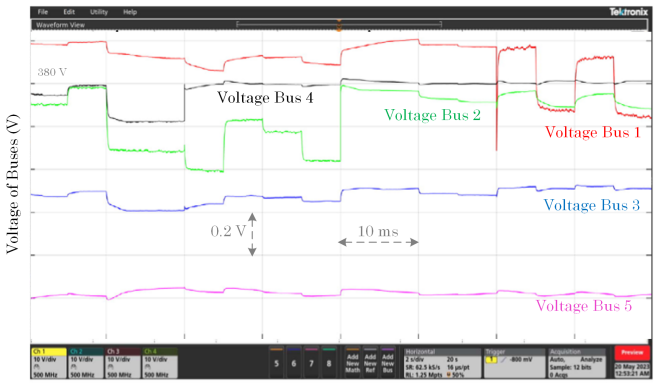

Fig. 5. Scenario 2 (communication impairment): Voltage profiles of buses during the experiment

a sample-and-hold mechanism, so delayed updates effectively increase the age of neighbor data seen by the consensus-based secondary layer.

Figure 5 shows the measured bus voltages during this scenario. Despite the combined effect of time-varying loads and stochastic delay, the voltages remain bounded around the nominal operating level. The largest excursions occur on Bus 1 during the most demanding load intervals, while the other buses exhibit smaller deviations and recover toward their pre-disturbance levels. These traces are consistent with the intended behavior of the proposed architecture: transient corrections are supported by the bounded trim layer, while the supervisor and controller-bank selection avoid rapid or unsafe parameter changes when communication quality degrades.

C. Quantitative Results Summary

To complement the voltage traces in Figs. 4 and 5, Table II summarizes voltage-regulation, SoC-sharing, and communication outcomes over the 80 s HIL runs. The RMS and peak voltage errors (e_{rms}, $e_{\max}$) are computed with respect to V_{ref} (p.u./%), and the settling time T_{set} is measured to the band $\pm\epsilon_v$ with $\epsilon_v = 0.002$ p.u. after each disturbance segment; the reported T_{set} is the worst-case settling time within the scenario. The SoC metric Δ_{soc} is the maximum SoC spread across units over the run. The communication reduction R_{comm} is computed relative to periodic communication with the same sampling rate and exchanged variables. As expected, Scenario 2 (time-varying loads with stochastic delay) produces larger voltage excursions and longer worst-case settling time than Scenario 1, since delayed neighbor information reduces the effective coordination bandwidth of the consensus layer. Nevertheless, the proposed event-triggered policy maintains bounded regulation while reducing message rate by 30-45% relative to the periodic baseline, and the SoC spread remains limited in both scenarios.

TABLE II
QUANTITATIVE SUMMARY OVER $T = 80$ S (S1: SCENARIO 1, S2: SCENARIO 2).

Scen.	e_{rms} (%)	$e_{\max}$ (p.u.)	T_{set} (s)	Δ_{soc} (%)	R_{comm} (%)
S1	0.07	0.0020	2.6	1.8	45
S2	0.12	0.0100	4.8	2.6	30

V. CONCLUSION AND FUTURE WORKS

This paper presented a structured secondary control strategy for islanded DC microgrids that remains effective when the coordination layer is carried by wireless links with delay, loss, and bandwidth limits. The method combines four elements: a consensus-based secondary integrator for voltage restoration and SoC sharing, an event-triggered communication rule with hysteresis and explicit lower and upper bounds of inter-event times, a finite controller bank with eight prevalidated parameter modes, and a supervisor that limits mode changes and provides rollback to a conservative safe mode. In addition, a fast bounded trim layer applies small reference micro-adjustments at each control tick to improve transient response while keeping the slow dynamics inside tested operating bounds. Experimental HIL studies on a 380 V DC microgrid with 10–200 ms delay and up to 15% packet loss demonstrate reduced transmission rates relative to periodic exchange while maintaining voltage regulation and SoC balancing across representative scenarios, and improved robustness during communication impairment.

Future work will extend the framework in two directions. First, larger-scale studies with higher node counts and varying graph topologies will be used to assess scalability more systematically. Second, the classifier and controller bank will be enriched to cover broader operating regions, including plug-and-play operation and stronger constant-power-load effects.

REFERENCES

[1] M. A. Jarrahi and V. Abolghasemi, "A power control and management framework for integration of pv-based dc microgrids with battery storages and supercapacitors," *IEEE Open Access Journal of Power and Energy*, 2025.

[2] V. F. Pires, A. Pires, and A. Cordeiro, "Dc microgrids: benefits, architectures, perspectives and challenges," *Energies*, vol. 16, no. 3, p. 1217, 2023.

[3] M. A. Jarrahi, F. Roozitalab, M. M. Arefi, M. S. Javadi, and J. P. Catalao, "Dc microgrid energy management system containing photovoltaic sources considering supercapacitor and battery storages," in *2020 International Conference on Smart Energy Systems and Technologies (SEST)*. IEEE, 2020, pp. 1–6.

[4] S. A. Alavi, K. Mehran, V. Vahidinasab, and J. P. Catalão, "Forecast-based consensus control for dc microgrids using distributed long short-term memory deep learning models," *IEEE Transactions on Smart Grid*, vol. 12, no. 5, pp. 3718–3730, 2021.

[5] F. S. Al-Ismail, "A critical review on dc microgrids voltage control and power management," *IEEE Access*, vol. 12, pp. 30 345–30 361, 2024.

[6] X. Jin, Y. Shen, and Q. Zhou, "A systematic review of robust control strategies in dc microgrids," *The Electricity Journal*, vol. 35, no. 5, p. 107125, 2022.

[7] K. Etivand and M. Kalantar, "Dynamic event-triggered fixed-time distributed secondary control for dc microgrids under control signal uncertainty," *International Journal of Electrical Power & Energy Systems*, vol. 174, p. 111449, 2026.

[8] J. Shi, W. Xue, and K. Li, "Reinforcement learning-driven control strategies for dc flexible microgrids: Challenges and future," *Energies*, vol. 19, no. 3, p. 648, 2026.

[9] B. Abdolmaleki and G. Bergna-Diaz, "Distributed control and optimization of dc microgrids: A port-hamiltonian approach," *IEEE Access*, vol. 10, pp. 64 222–64 233, 2022.

[10] M. A. Jarrahi, M. J. Nasero, H. Samet, T. Ghanbari, and K. Mehran, "An alienation-coefficient based fault detection method for dc microgrid," *International Journal of Electrical Power & Energy Systems*, vol. 175, p. 111626, 2026.

[11] S. A. Alavi, A. Rahimian, K. Mehran, and V. Vahidinasab, "Multi-layer event-based distributed control system for dc microgrids with non-uniform delays and directional communication," *IET Generation, Transmission & Distribution*, vol. 16, no. 2, pp. 267–281, 2022.